EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S6	3014	(phase delay) near interpolat$4 (phase delay) adj interpolat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 12:17
S7	295842	switch near3 (power supply)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 10:31
S8	35525	switch near3 (ground)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 10:31
S9	202	inverter same S7 same S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 10:37
S14	328	S6.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 11:45
S16	1	S6 same tri adj state near2 inverter	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 10:47
S17	15	S6 and tri adj state near2 inverter	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 13:20
S24	8	S6 and tri adj state near2 buffer	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 11:17
S36	159	fukushi.in. and fujitsu.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 11:58

EAST Search History

S37	1	S36 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 11:57
S40	98	(buffer inververter) same S7 same S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/13 12:21
S46	5112	tri adj state near2 (buffer inverter)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 13:21
S51	370	S46 and (delay phase) with (correction adjustment compensation)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 13:36
S58	142	floating adj gate same temperature same capacitor	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 14:08
S59	142	S58 and temperature	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 14:08
S60	47	S58 and (vref reference near2 voltage)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/13 14:08
S90	3043	pmos with large with threshold nmos with (small low threshold) with inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/12/14 09:57
S91	318	pmos with large with threshold nmos with (small low) near3 threshold with inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/12/14 09:59
S92	50	pmos near3 larg$4 near3 size near3 nmos	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/12/14 10:01
S93	53	pmos near3 larg$4 near3 nmos with inverter	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2007/12/14 10:04

EAST Search History

S97	302	skewed with inverter	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 10:08
S100	69	inverter with switch with (power supply vcc) with (clock clk clk1 clk2) with gate	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 10:38
S108	187	short adj circuit near3 (stop$4 prevent$4) with (inverter buffer)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:49
S115	52	interpolat$4 with (stop$4 prevent$4) with (inverter buffer)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:50
S116	4	interpolat$4 with (stop$4 prevent$4) with (short adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:15
S124	15	phase adj blend$4 and (buffer inverter) with (power supply ground vdd vss vcc gnd)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:13
S126	213	phase adj blend$4 and (buffer inverter)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:13
S127	355	(inverter buffer) with (stop$4 prevent$4) with (short adj circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:45
S128	168	S127 not S108	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:45
S135	3	S134 same switch with (power supply vdd vcc vss ground gnd)	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:55
S137	552	inverter with first adj clock same inverter with second adj clock	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 12:57